REMARKS

Claims 1 - 4 are pending. Claims 1, 2, and 4 have been amended. No new matter has been introduced. Reexamination and reconsideration of the application are respectfully requested.

In the October 29, 2005 Office Action, the Examiner objected to claim 2 as being dependent on a rejected base claim, but indicated it would be allowable if rewritten in independent form including all of the limitations of the base claim and intervening claims. The applicant has rewritten claim 2 to include all of the limitations of the base claim, i.e., claim 1. Accordingly, the applicant respectfully submits that claim 2 is in condition for allowance.

The Examiner objected to claims 1 and 4 for informalities. The applicant has amended claims 1 and 4 to address these informalities and respectfully submits that the Examiner's objection be withdrawn.

The Examiner rejected claims 1, 3, and 4 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,088,812 to Houg ("the Houg reference"). This rejection is respectfully traversed.

Claim 1 distinguishes over the cited references. The Houg reference does not disclose, teach, or suggest the circuit of claim 1.

> A digital signal delay compensating circuit:
>
> a first semiconductor circuit device including a clock-signal generating circuit and a data processing circuit for outputting a data signal in synchronism with a clock signal generated by the clock-signal generating circuit; and
>
> a second semiconductor circuit device to which the data signal output from the first semiconductor circuit device is inputted and which processes the data signal in synchronism with the clock signal,
>
> **wherein the clock signal to be supplied from the first semiconductor circuit device to the second semiconductor circuit**

device is fed back to the data processing circuit, and the fed-back clock signal is used as a clock signal at the time of outputting the data signal.

Claim 1 distinguishes over the Hong reference. The Examiner states that the Hong reference discloses that the clock signal to be supplied from the first semiconductor circuit device to the second semiconductor circuit device is fed back to the data processing circuit [134] and the fed-back clock signal is used as a clock signal at the time of outputting the data signal. *(Office Action, page 3)*. The applicant respectfully disagrees with Examiner.

In the Hong reference, the clock signal 148 is transmitted to the sequential storage device 102 at input 113, the control delay circuit 104 at input 120, the slack register 108 at input 134, and the receiver 112 at 152. *(Fig. 2, column 2, line 66- col. 3, line 49)*. In other words, the clock signal is directly fed to all of the above-identified inputs. There is no disclosure that the clock signal is fed-back to a data processing circuit. The Hong reference discloses that an IRDY# ready signal (flow control signal) is fed back to the control delay circuit. The flow control signal controls the flow out of the sequential storage device. By asserting the flow control, the receiver indicates that it will read the data item at multiplexer output 146 in response to the next clock trigger. *(Col. 3, line 57 to col. 4, line 1)*. The flow control signal is sent to a control data circuit (which the Examiner states is part of the data processing circuit) and there is no fed back clock signal.

The Hong reference does not disclose, teach, or suggest a digital signal delay compensating circuit **wherein the clock signal to be supplied from the first semiconductor circuit device to the second semiconductor circuit device is fed**

back to the data processing circuit, and the fed-back clock signal is used as a clock signal at the time of outputting the data signal. As discussed above, the Hong reference does not disclose that the clock signal is fed back to the data processing circuit because it does not disclose a clock signal being fed back to any device and specifically not a data processing circuit. Accordingly, applicant respectfully submits that claim 1 distinguishes over the Hong reference.

Claim 3 depends on independent claim 1. Accordingly, applicant respectfully submits that claim 3 distinguishes overt the Hong reference for the same reasons as those discussed above in regard to claim 1.

Claim 4 distinguishes over the cited references. Claim 4 recites:

> A digital signal delay compensating circuit comprising:
> a storage device capable of writing data therein; and
> a semiconductor circuit device including an access timing signal generating circuit for writing the data in the storage device and configured to write the data in the storage data,
> wherein **an access timing signal to be supplied from the semiconductor circuit device to the storage device is fed back to the semiconductor circuit device**, and **a reference signal for allowing the semiconductor circuit device to output data to be written in the storage device is made active in a case where both the fed-back signal and a signal outputted from the access timing signal generating circuit are active.**

The Houg reference does not disclose, teach, or suggest the digital signal delay compensating circuit of claim 4. The Examiner states that the access timing signal fed back to the semiconductor circuit device is input at reference numeral 134. *(Office Action, page 3)*. The applicant disagrees because the clock signal the Examiner is pointing to is input directly to a slack register 108. In other words, the signal flows directly from input 148 to input 134. It is not **fed back to the semiconductor circuit device**, as recited in claim 4. Further, the Hong reference does not disclose that when the clock signals are active that a reference signal, i.e., the flow control signal IRDY#, is also active. Specifically, the timing diagrams of the Fig. 3 of the Houg reference do not show that the reference signal is active when the clock signal is active. Therefore, the Houg reference does not disclose a digital signal delay compensating circuit wherein **a reference signal is made active in a case where both the fed-back signal and a signal outputted from the access timing signal generating circuit are active**, as is recited in claim 4. Accordingly, applicant respectfully submits that claim 4 distinguishes over the Houg reference.

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Applicant believes that the claims are in condition for allowance, and a favorable action is respectfully requested. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call either of the undersigned attorneys at the Los Angeles telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the Examiner believe that such a telephone conference would advance prosecution of the application.

Respectfully submitted,

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